# IR and Thermal Modeling

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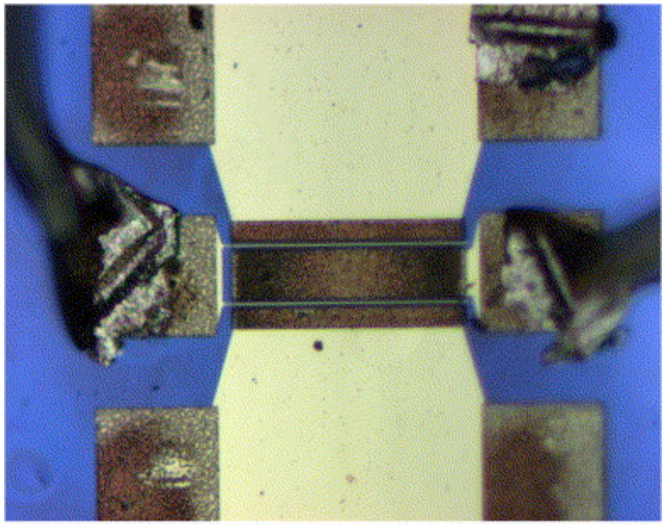
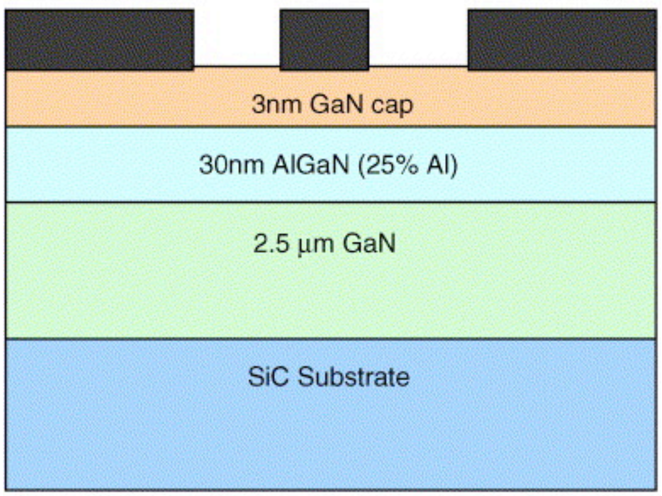
# μ-Raman(collaboration with Jaime Freitas and Jihyun Kim)

- Contact-free and non-destructive.
- Spatial resolution typically ≤ 1 μm, compared with conventional infrared technique (IR) with15μm spatial resolution. IR is not suitable for current advanced device designs because the channel spacing is normally less than 5 μm.
- First order Raman Scattering spectroscopy can be directly measure device temperature with  high spatial resolution and has been previously used to access device temperatures by monitoring phonon frequency shift with temperature.
- “Effective temperature measurements of AlGaN/GaN-based HEMT under various load lines using micro-Raman technique”, Solid-State Electron., 50, 408(2006),Jihyun Kim, Jr., J.A. Freitas, J. Mittereder, R. Fitch, B.S. Kang, S.J. Pearton and F. Ren.

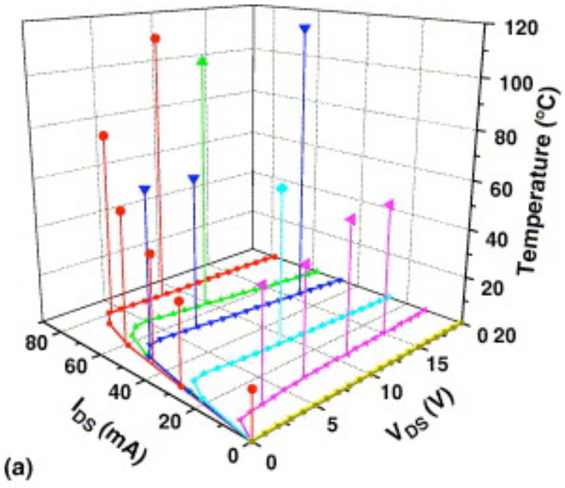
# Raman scattering of GaN HEMTs



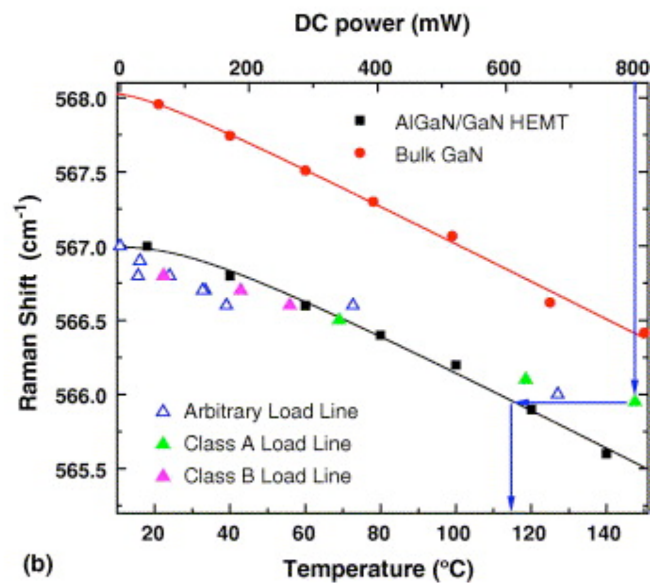
(a)




(b)



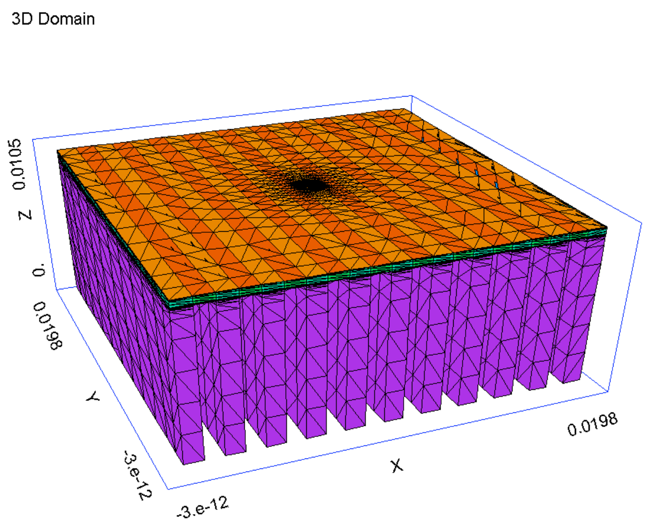

(a)

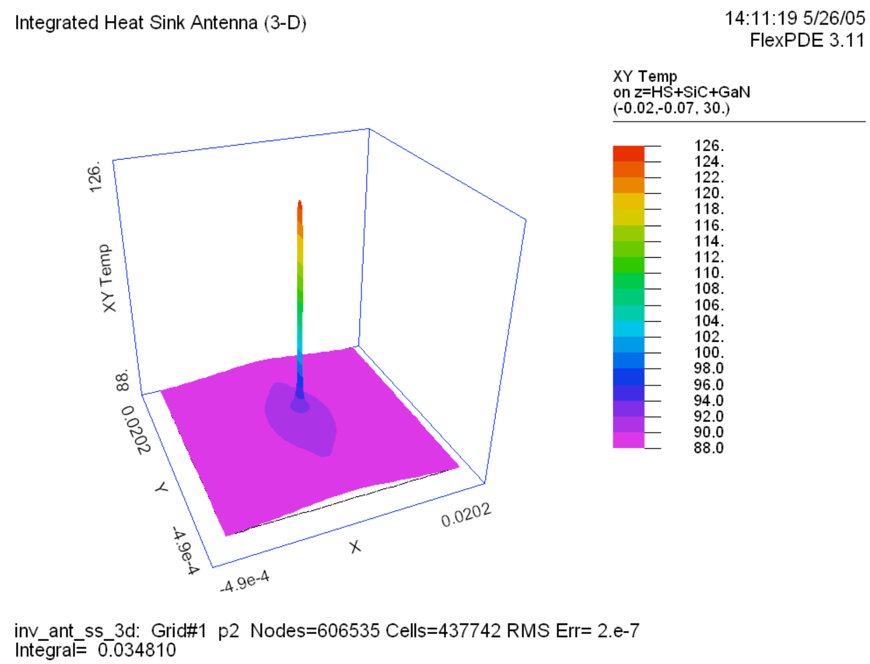



(b)

# Thermal Simulations

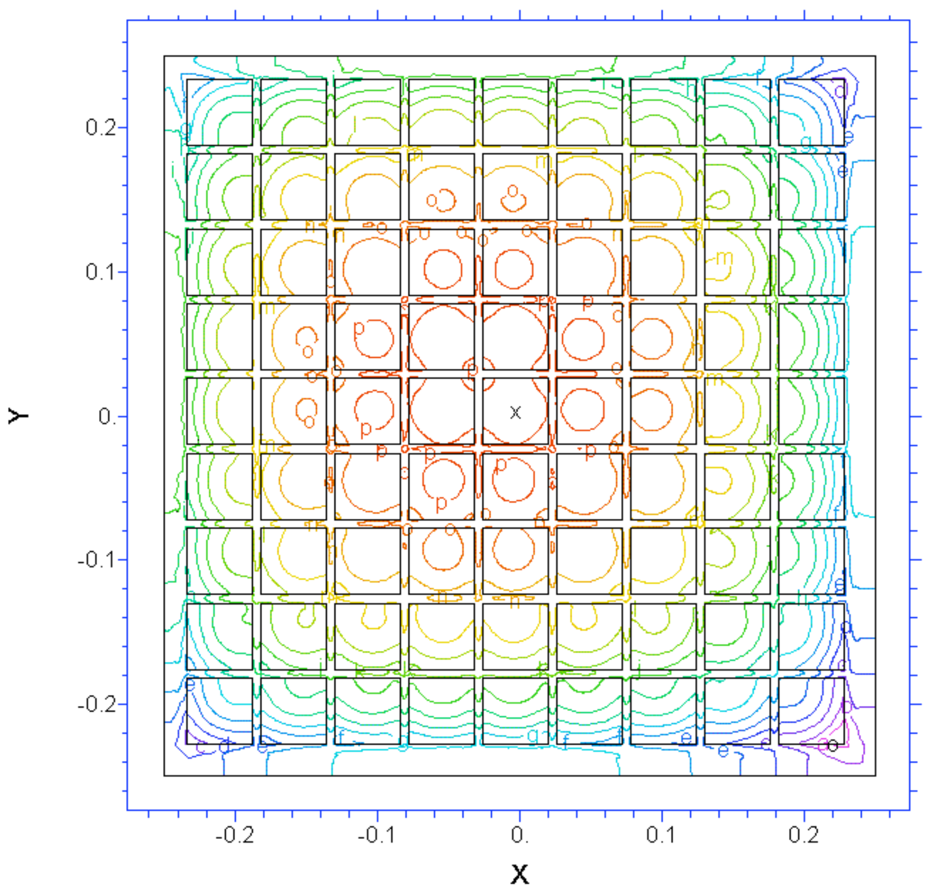
- Use finite element modeling to optimize package design
- Most important factors in thermal management: heat transfer at the system boundaries and substrate thickness



# Top of the chip

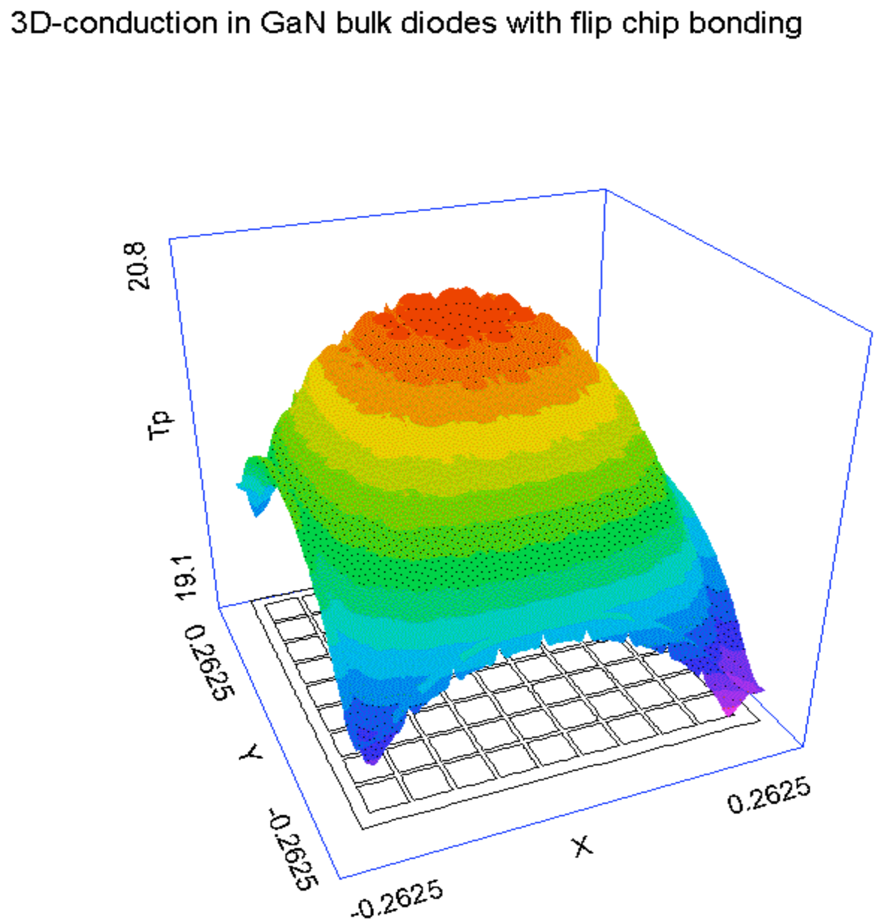
3D-conduction in GaN bulk diodes with flip chip bonding



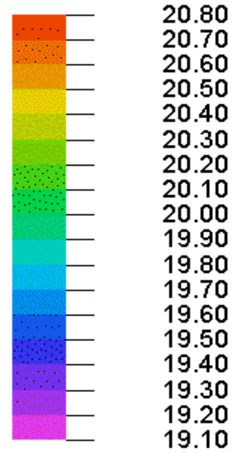

**Temperature rise from room temperature (°C)**

| | |
|---|---|
| max | 20.78 |
| p : | 20.70 |
| o : | 20.60 |
| n : | 20.50 |
| m : | 20.40 |
| l : | 20.30 |
| k : | 20.20 |
| j : | 20.10 |
| i : | 20.00 |
| h : | 19.90 |
| g : | 19.80 |
| f : | 19.70 |
| e : | 19.60 |
| d : | 19.50 |
| c : | 19.40 |
| b : | 19.30 |
| a : | 19.20 |
| min | 19.15 |

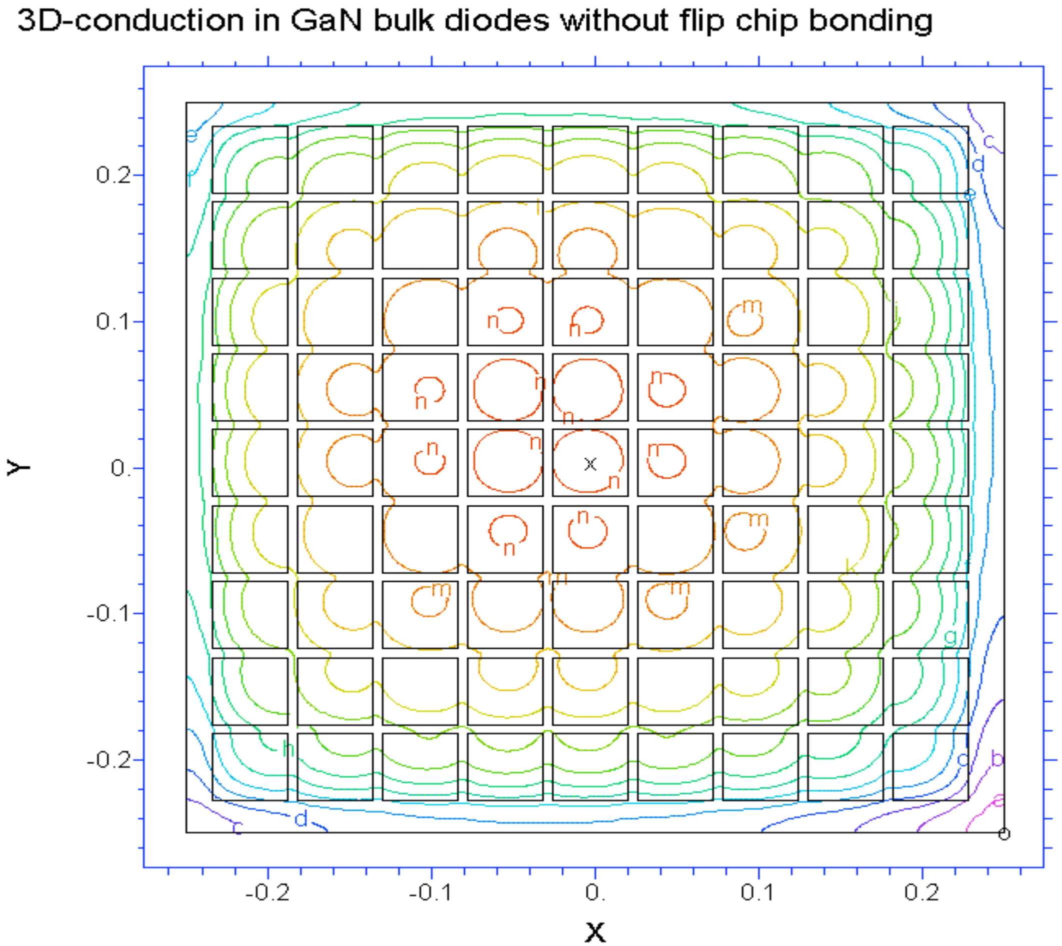
# Top of the chip




**Temperature rise from room temperature (°C)**



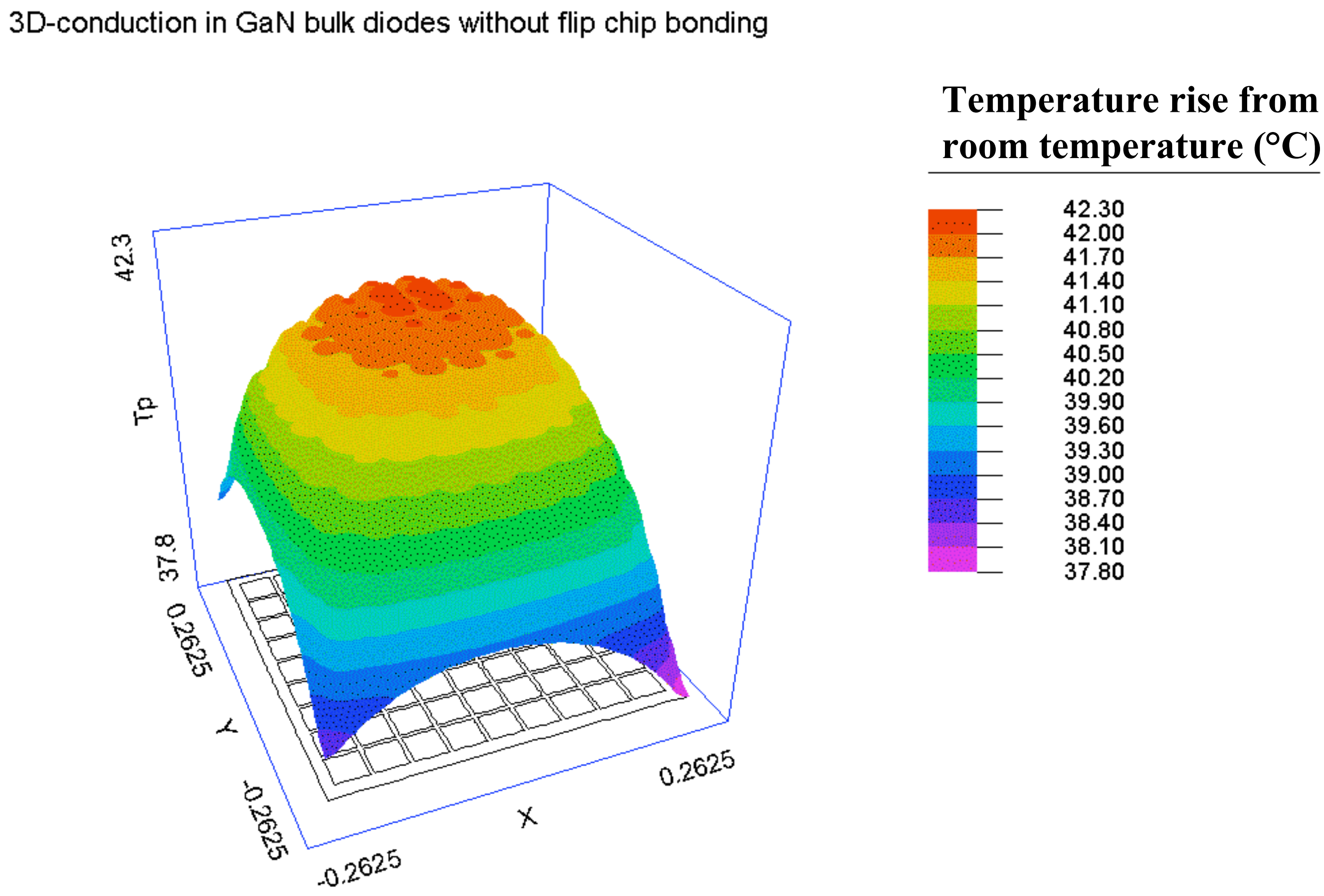
# Top of the chip




**Temperature rise from room temperature (°C)**

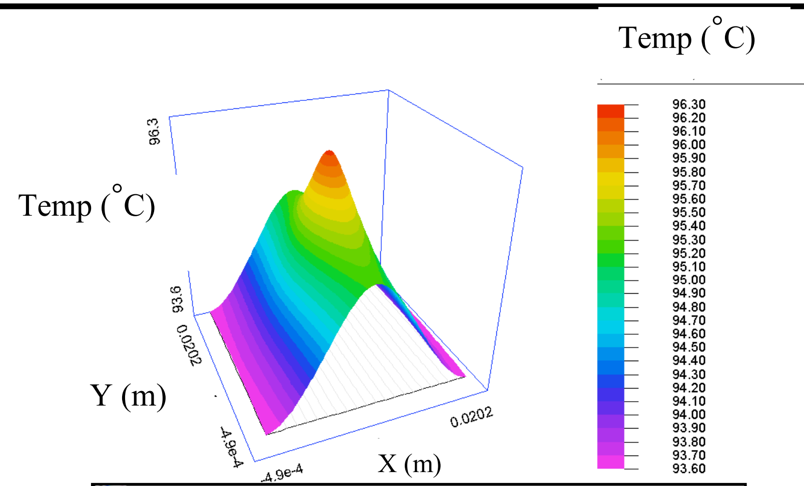
| | |
|---|---|
| max | 42.13 |
| n : | 42.00 |
| m : | 41.70 |
| l : | 41.40 |
| k : | 41.10 |
| j : | 40.80 |
| i : | 40.50 |
| h : | 40.20 |
| g : | 39.90 |
| f : | 39.60 |
| e : | 39.30 |
| d : | 39.00 |
| c : | 38.70 |
| b : | 38.40 |
| a : | 38.10 |
| min | 37.96 |

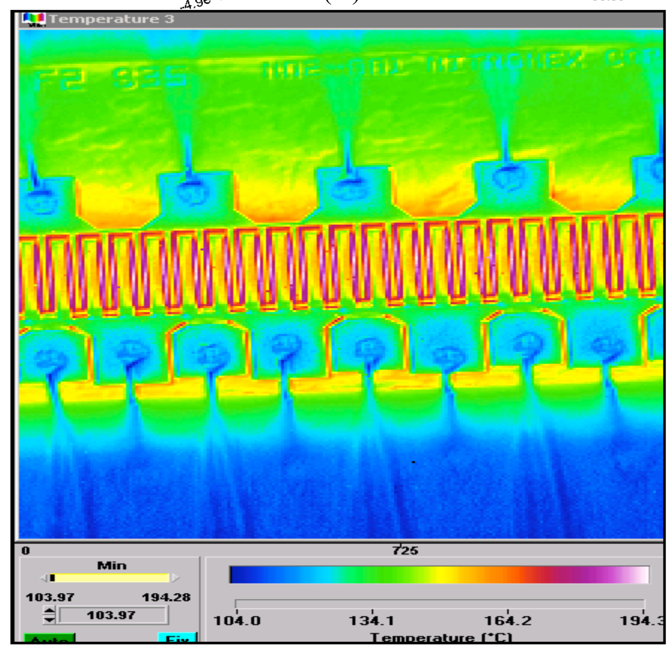
# Top of the chip



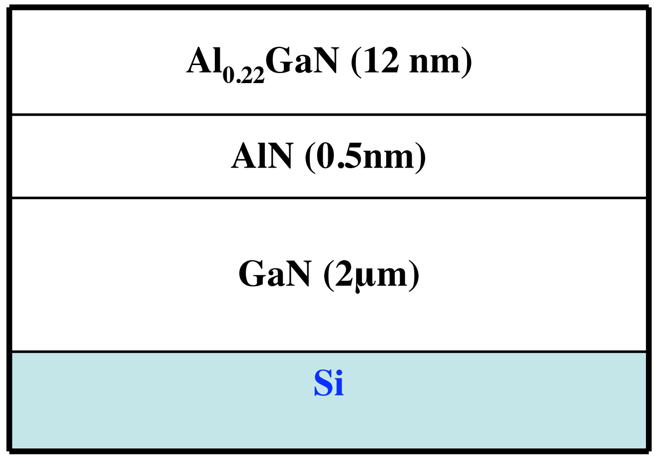
# Thermal Simulations and IR Imaging

- T(Junc) of power devices is often significantly hotter than T(stage)
- Accurate extraction of activation energy requires knowledge of the true channel temperature.
- We have extensive experience in estimating heat transfer even in complex structures
- Purchasing a high-resolution IR camera for direct imaging of the device operating temperature. We have collaborated with Nitronex on thermal imaging-a typical example is shown at right for a multi-finger power HEMT.



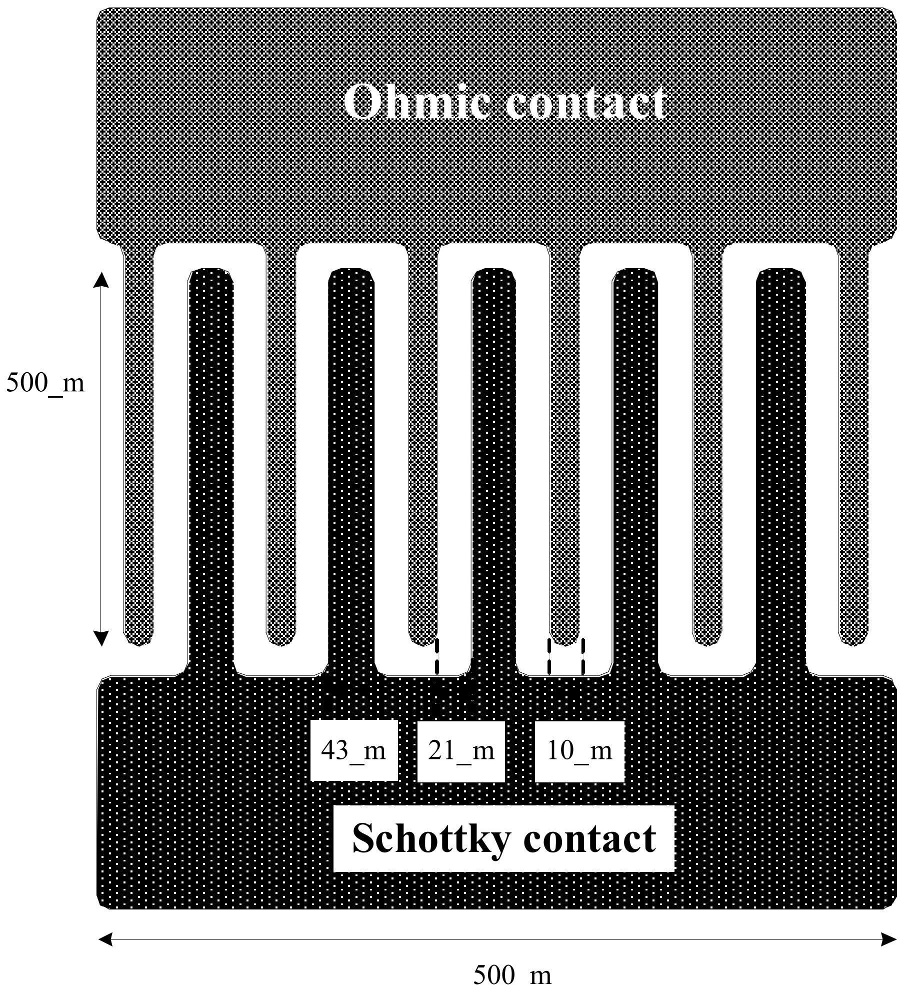



# Epilayer Structures of HEMT-collaboration with NCU in Taiwan




| | |
|---|---|
| Sheet carrier concentration ($1/cm^2$) | $-1.12 \times 10^{13}$ |
| Mobility ($cm^2/Vs$) | 1120 |
| Sheet resistance (ohm/sq) | 471.3 |

# Layout of 5-fingers SBD



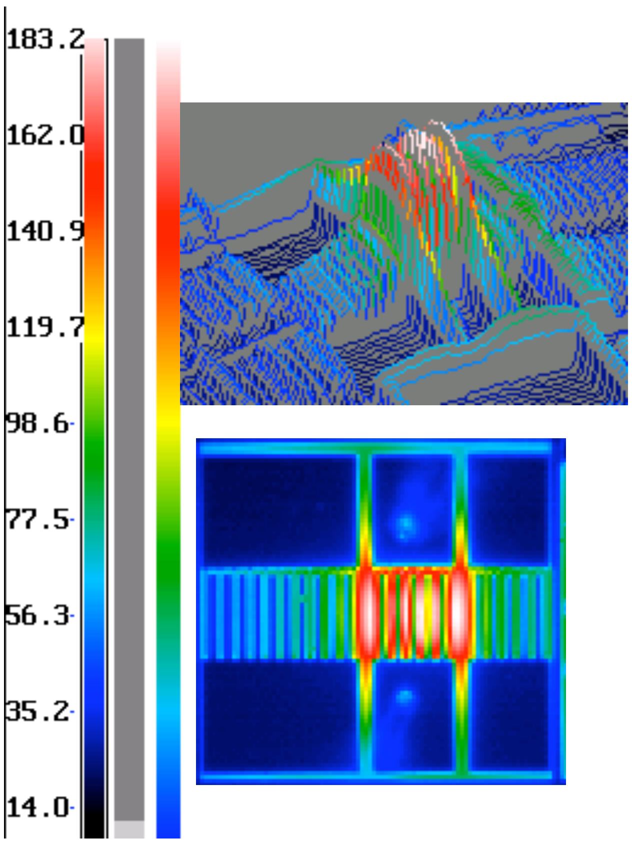

Process Flow:

1. Etch mesa (300nm depth)
2. Ohmic contact (2500nm thickness)
3. Schottky contact & pad (1.5µm thickness)

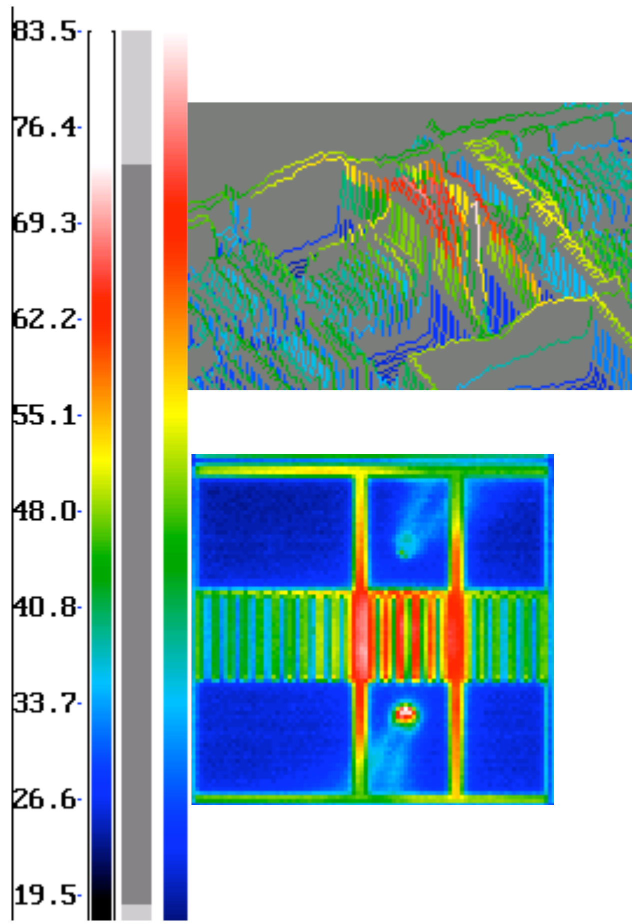
$V_{RB}$~200 V

# 3D Thermal Images

- On sapphire (4.2 W)

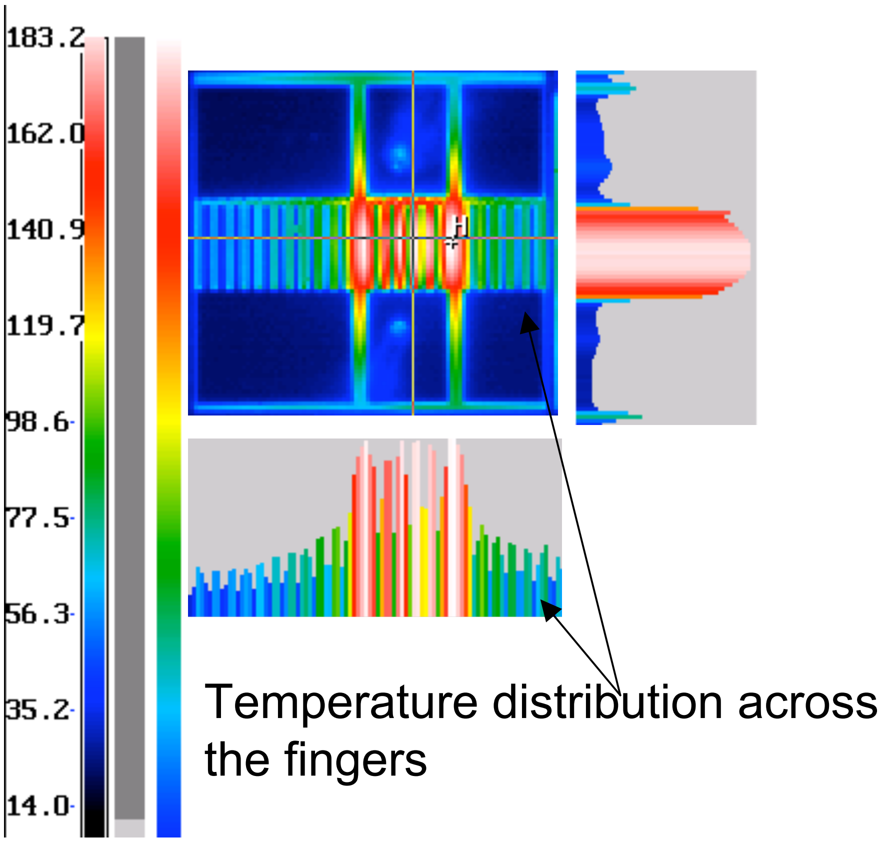



- On Si(11.8W)

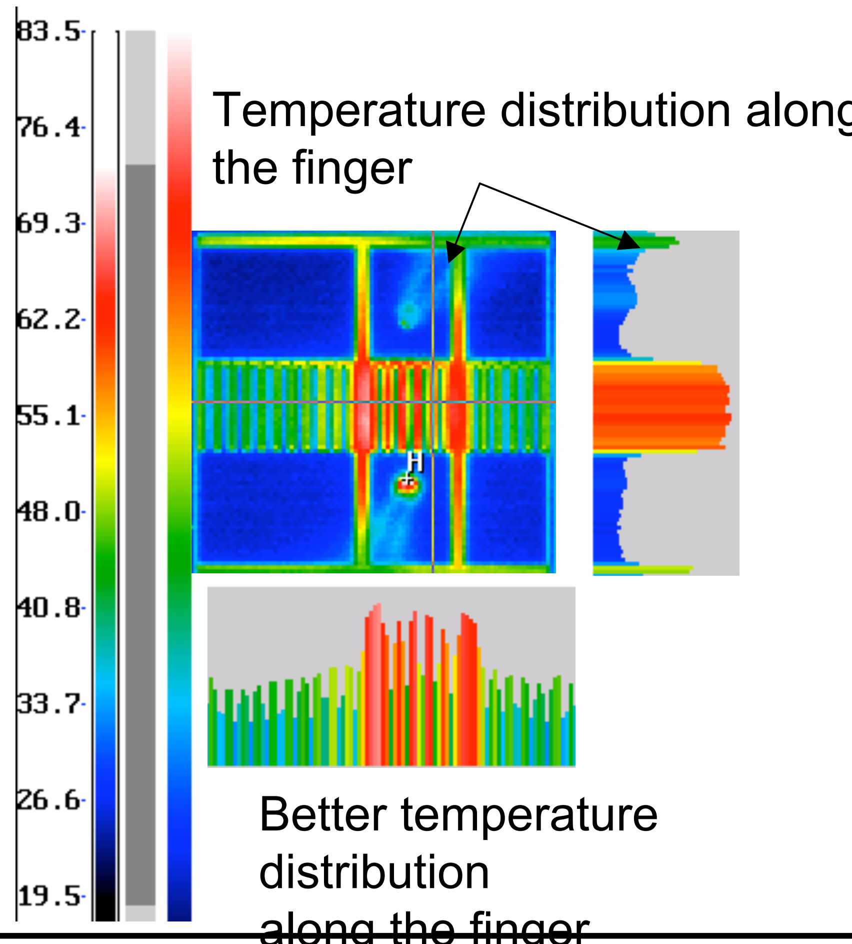


# Cross Sectional Thermal Images

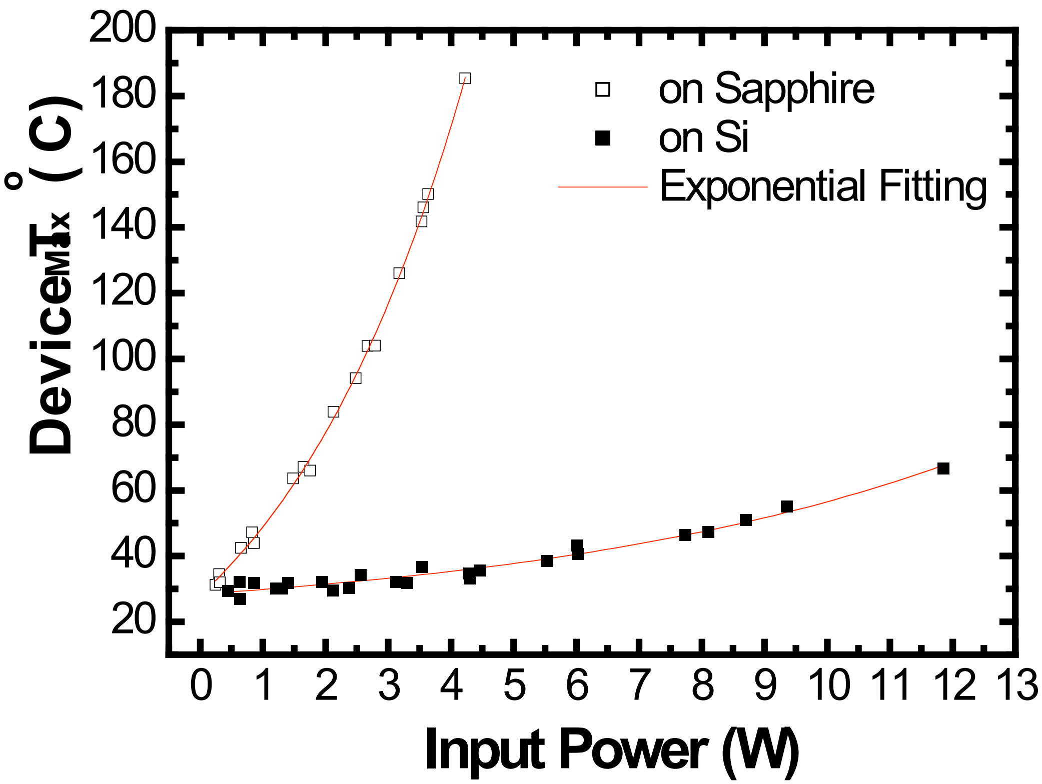
- On sapphire (4.2 W)




- On Si(11.8W)



# Temperature vs. input power




- 5 Fingers SBD (500 X 500 μ m$^2$)

  $L_{GD}$=21 μ m, $L_G$=43 μ m

  $L_D$=10 μ m, $W_G$=500 μ m